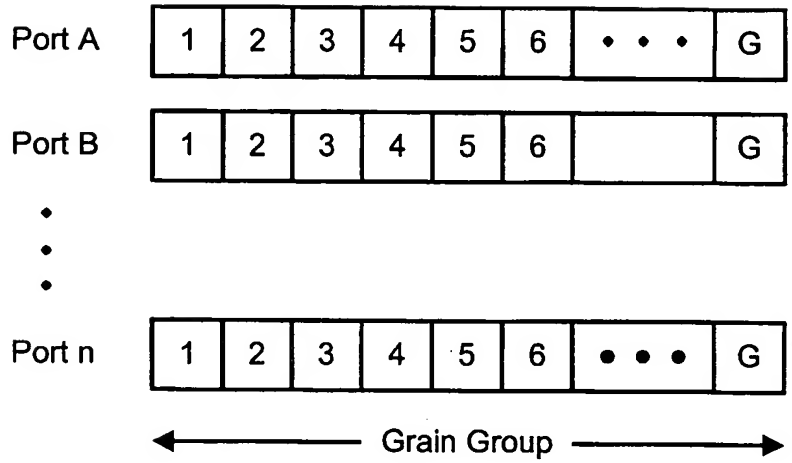


FIG. 1
PRIOR ART

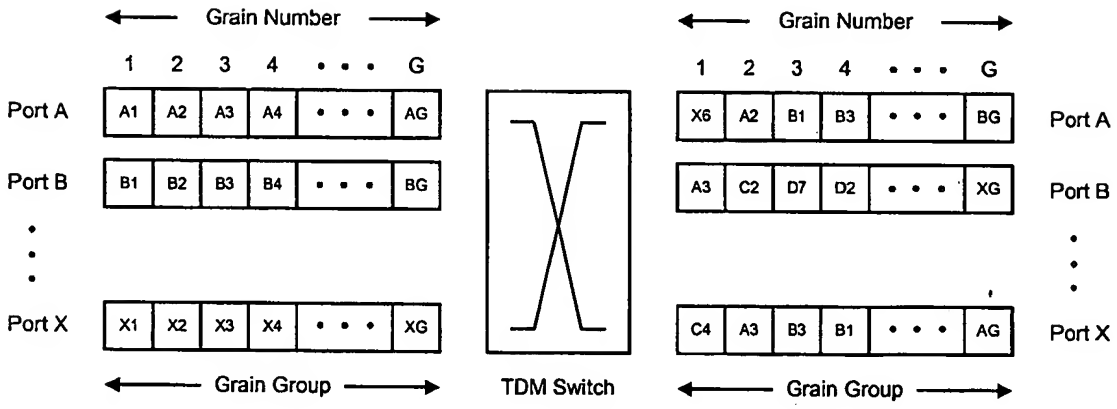
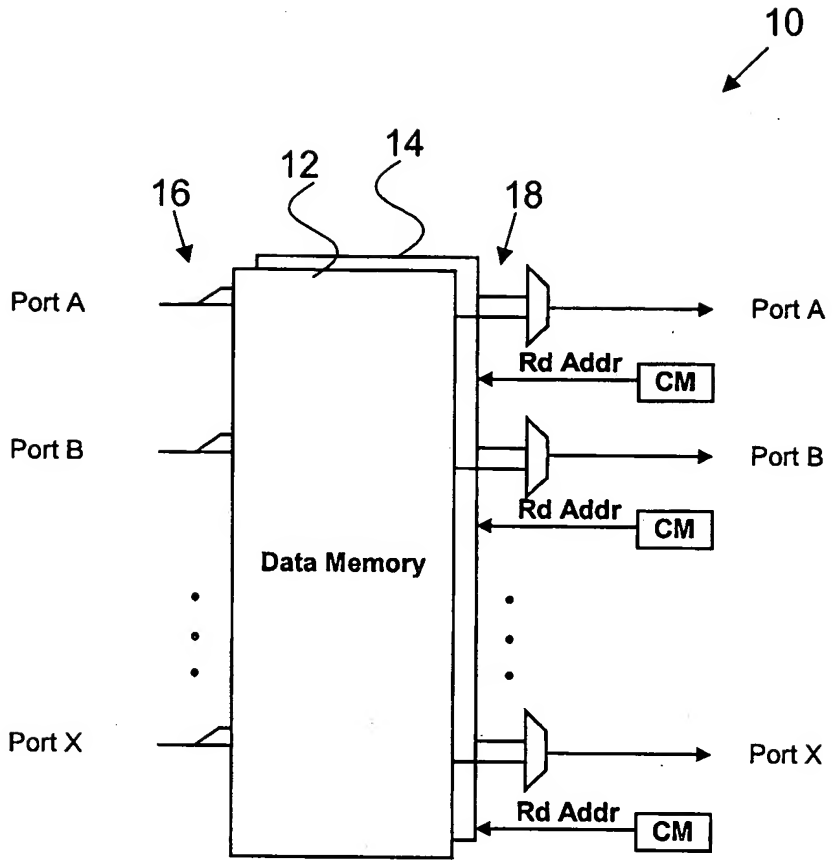


FIG. 2
PRIOR ART



CM: Connection Memory

FIG. 3
PRIOR ART

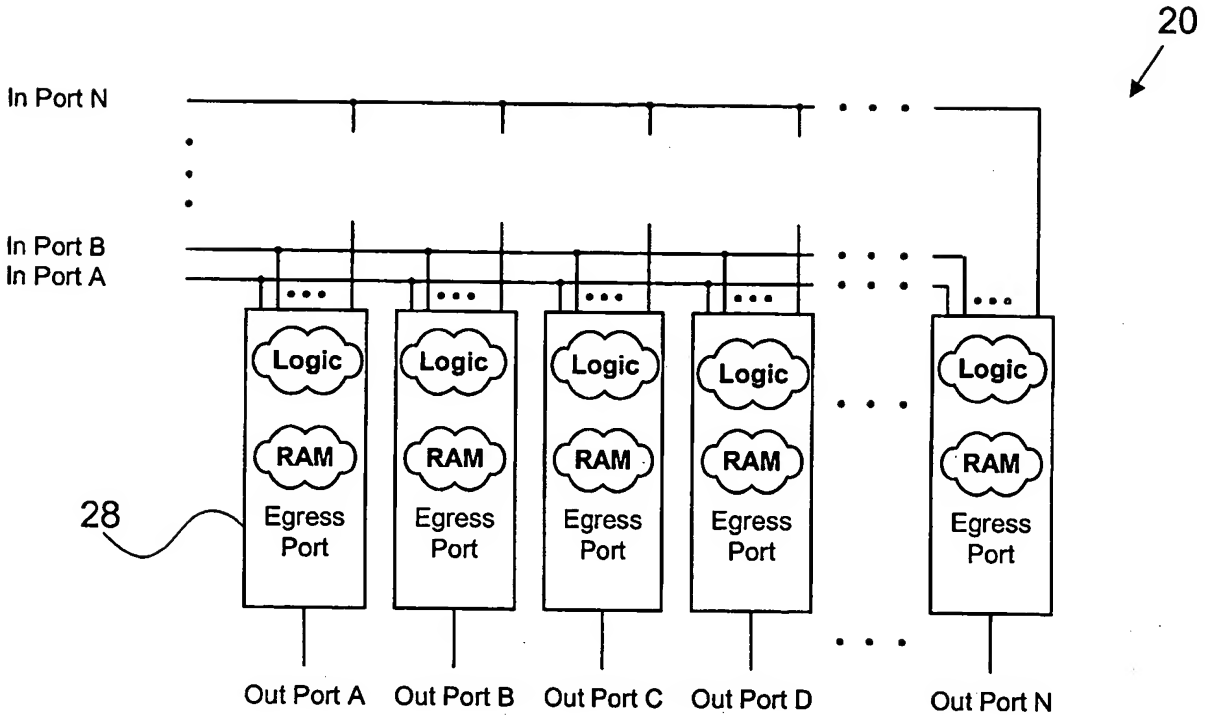


FIG. 4
PRIOR ART

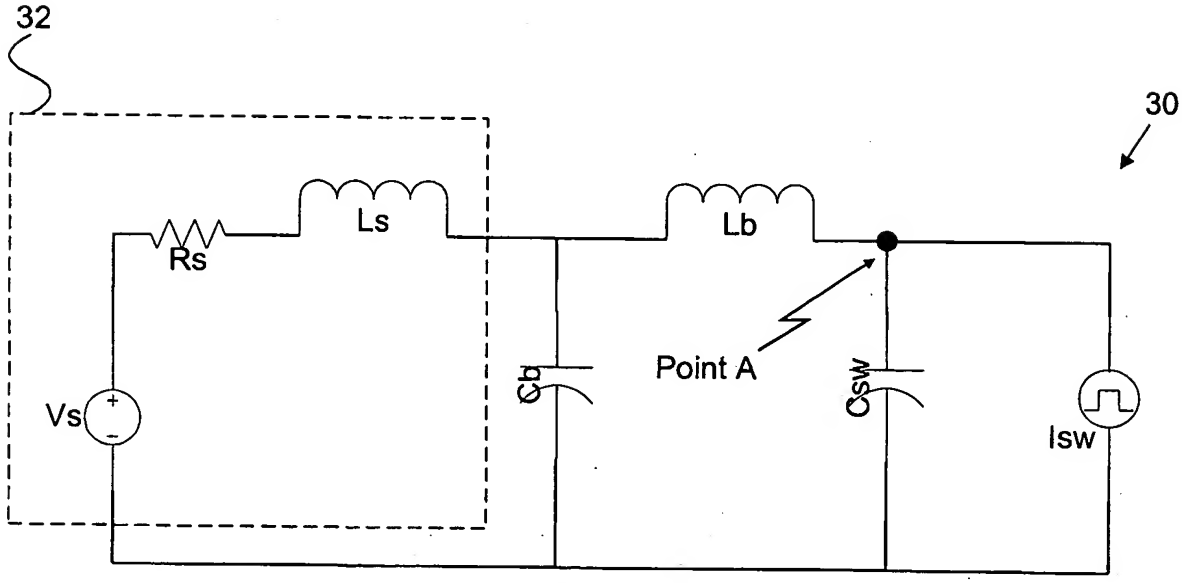


FIG. 5
PRIOR ART

Timeslots 1-48	Timeslots 49-96	Timeslot 97	Timeslots 98-144	Timeslots 144-4320
A1 ('hF6)	A2 ('h28)	J0 ('h??)	Z0 ('h00)	Payload
				Payload
				Payload
H1	H2	H3	H3	Payload
				Payload
				Payload
				Payload
				Payload
				Payload

FIG. 6
PRIOR ART

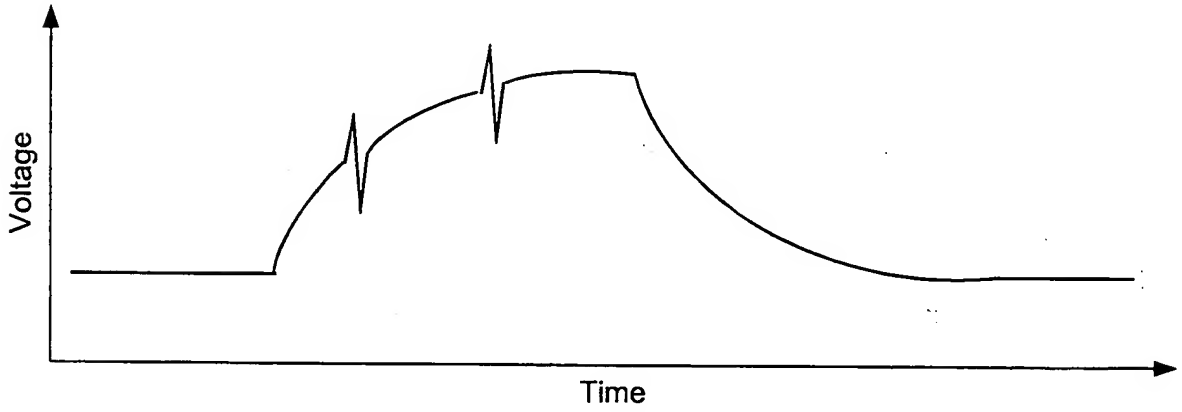


FIG. 7
PRIOR ART

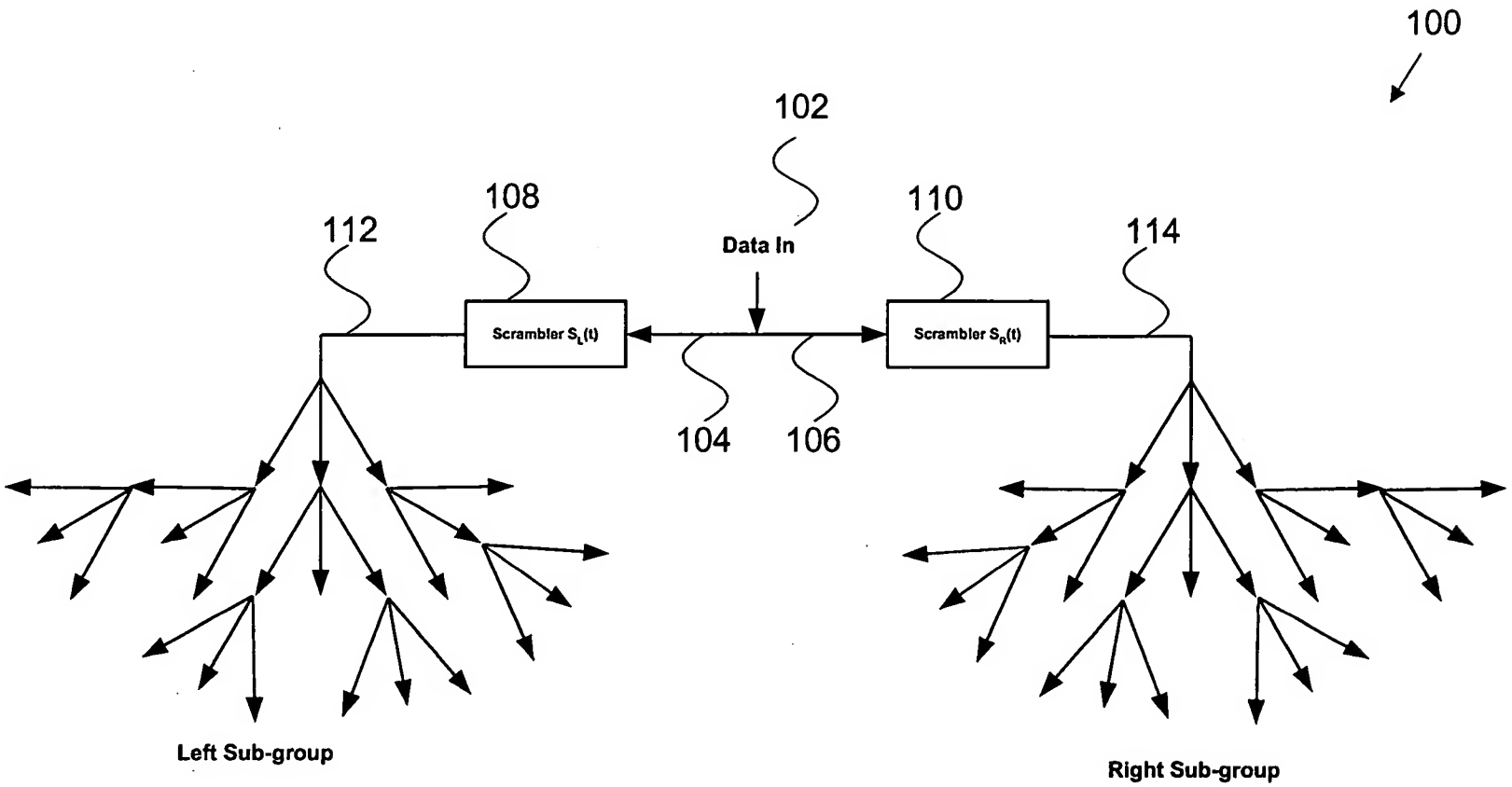

100
102
108
110
112
114
Data In
Scrambler $S_L(t)$
Scrambler $S_R(t)$
104
106
Left Sub-group
Right Sub-group

FIG. 8

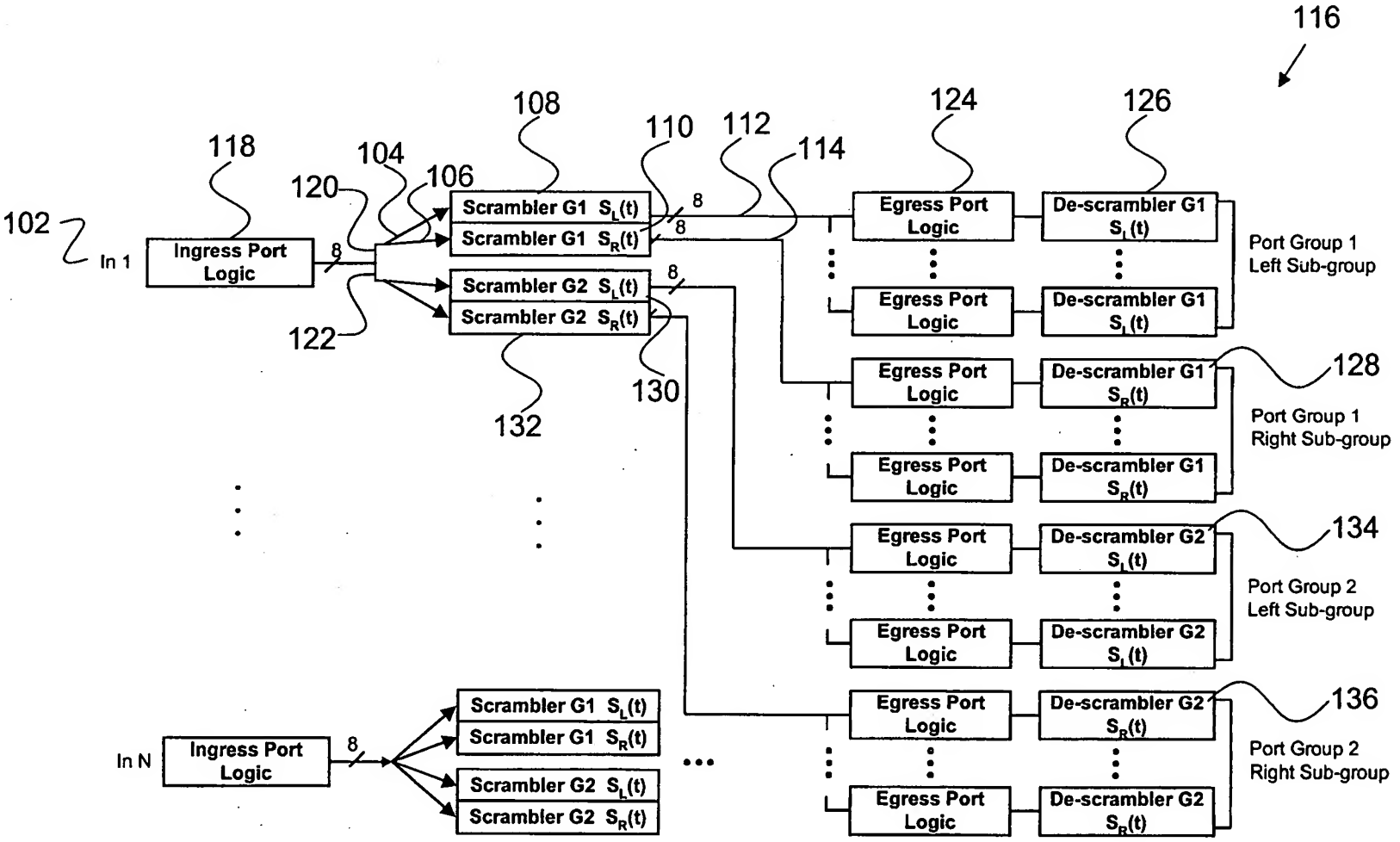

116
102
In 1
Ingress Port Logic
In N
Ingress Port Logic
118
120
104
106
108
110
112
114
122
130
132
124
126
128
134
136
8
Scrambler G1 $S_L(t)$
Scrambler G1 $S_R(t)$
Scrambler G2 $S_L(t)$
Scrambler G2 $S_R(t)$
Egress Port Logic
De-scrambler G1 $S_L(t)$
De-scrambler G1 $S_R(t)$
De-scrambler G2 $S_L(t)$
De-scrambler G2 $S_R(t)$
Port Group 1 Left Sub-group
Port Group 1 Right Sub-group
Port Group 2 Left Sub-group
Port Group 2 Right Sub-group

FIG. 9

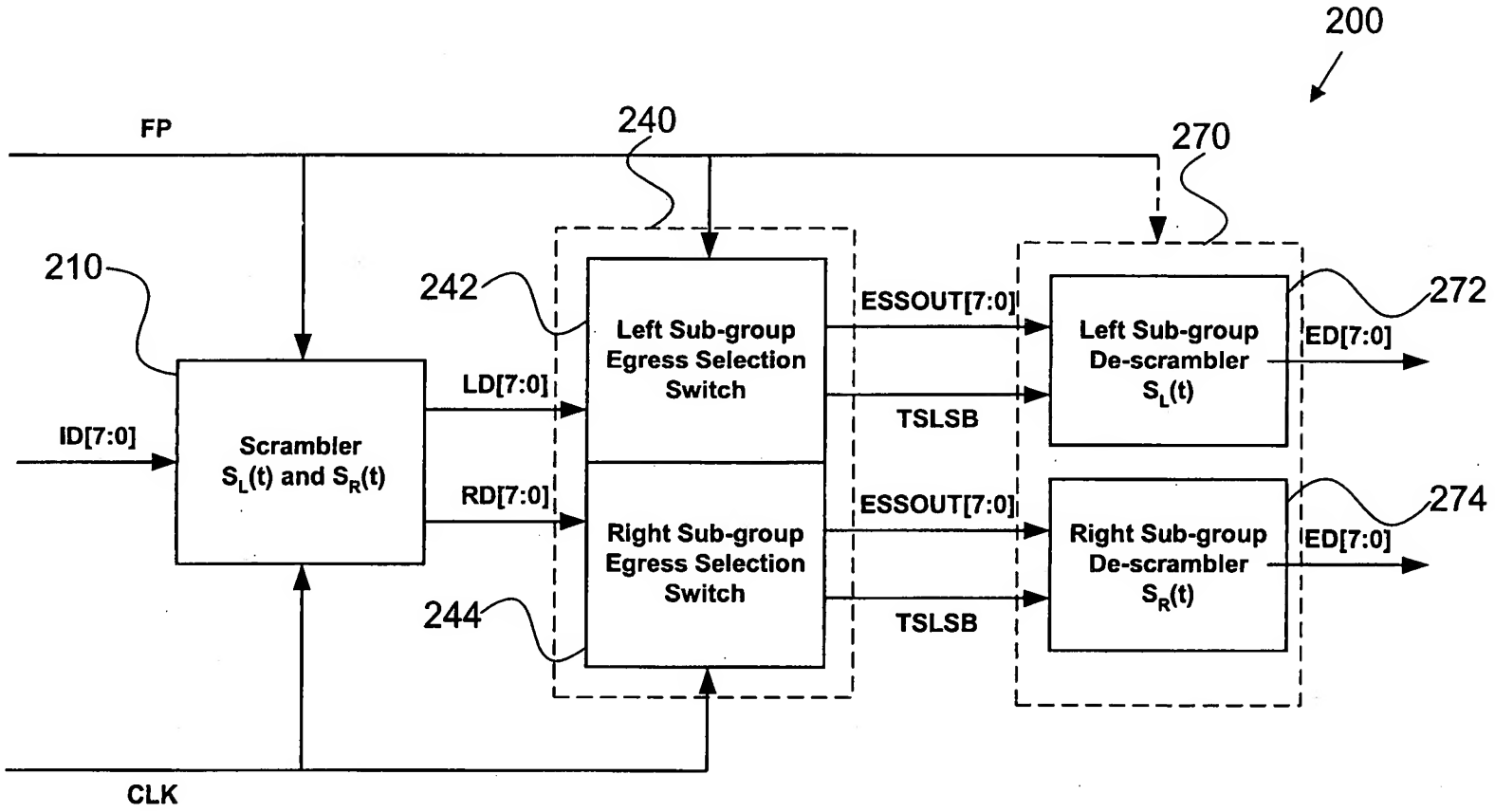

200
FP
240
270
210
242
Left Sub-group Egress Selection Switch
ESSOUT[7:0]
Left Sub-group De-scrambler $S_L(t)$
272
ED[7:0]
LD[7:0]
ID[7:0]
Scrambler $S_L(t)$ and $S_R(t)$
TSLSB
RD[7:0]
ESSOUT[7:0]
Right Sub-group De-scrambler $S_R(t)$
274
ED[7:0]
Right Sub-group Egress Selection Switch
244
TSLSB
CLK

FIG. 10

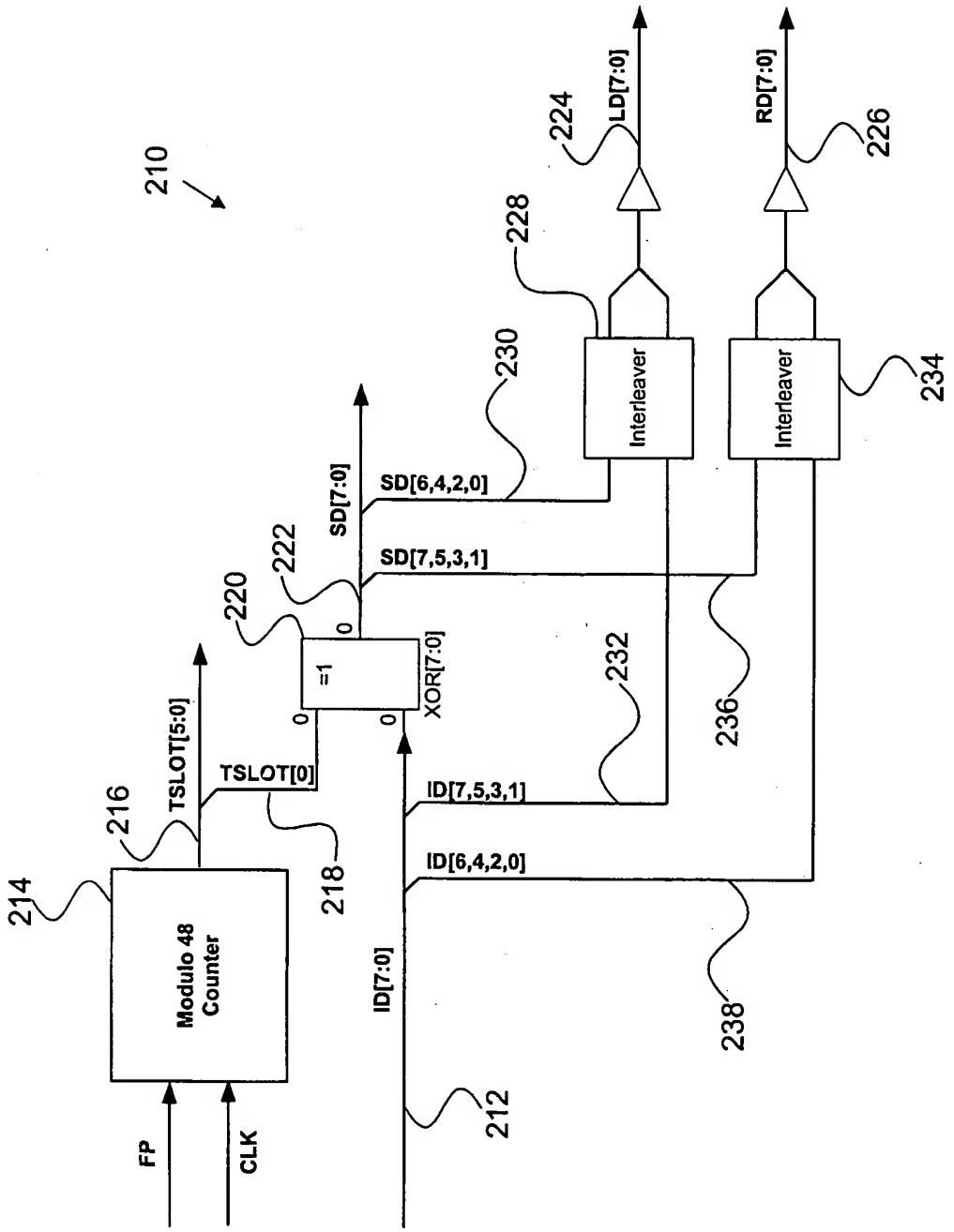

210
214
Modulo 48 Counter
216
TSLOT[5:0]
TSLOT[0]
218
FP
CLK
220
222
SD[7:0]
SD[6,4,2,0]
SD[7,5,3,1]
=1
XOR[7:0]
ID[7:0]
212
ID[7,5,3,1]
ID[6,4,2,0]
224
LD[7:0]
228
230
Interleaver
RD[7:0]
226
234
Interleaver
232
236
238

FIG. 11

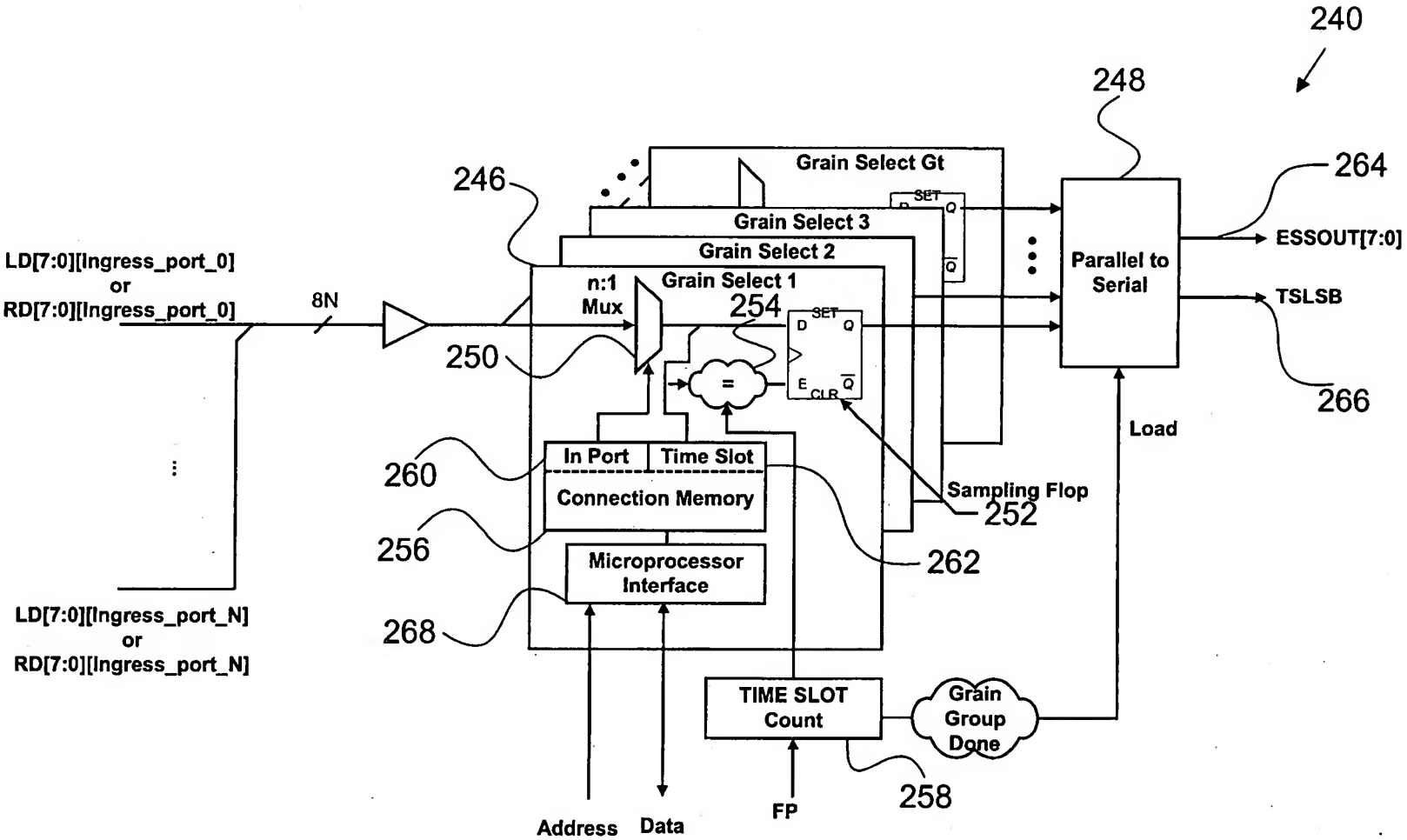

240
248
246
Grain Select Gt
Grain Select 3
Grain Select 2
Grain Select 1
n:1
Mux
254
250
LD[7:0][Ingress_port_0]
or
RD[7:0][Ingress_port_0]
8N
LD[7:0][Ingress_port_N]
or
RD[7:0][Ingress_port_N]
Parallel to
Serial
264
ESSOUT[7:0]
TSLSB
266
Load
In Port
Time Slot
Connection Memory
260
256
Microprocessor
Interface
268
Sampling Flop
252
262
TIME SLOT
Count
Grain
Group
Done
258
Address
Data
FP

FIG. 12

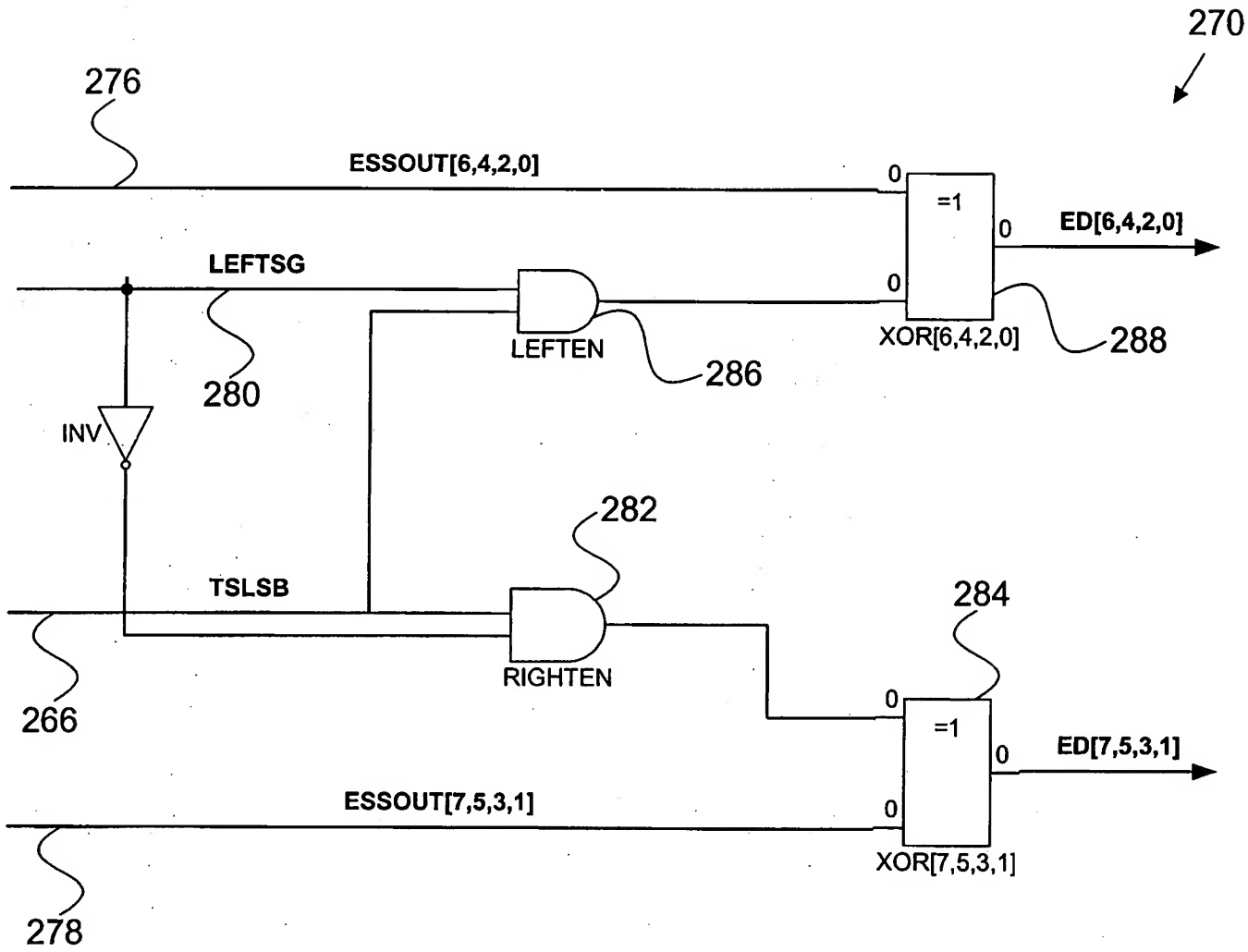

270
276
ESSOUT[6,4,2,0]
0
=1
0
ED[6,4,2,0]
LEFTSG
0
LEFTEN
286
XOR[6,4,2,0]
288
280
INV
282
TSLSB
284
266
RIGHTEN
0
=1
0
ED[7,5,3,1]
ESSOUT[7,5,3,1]
0
XOR[7,5,3,1]
278

FIG. 13

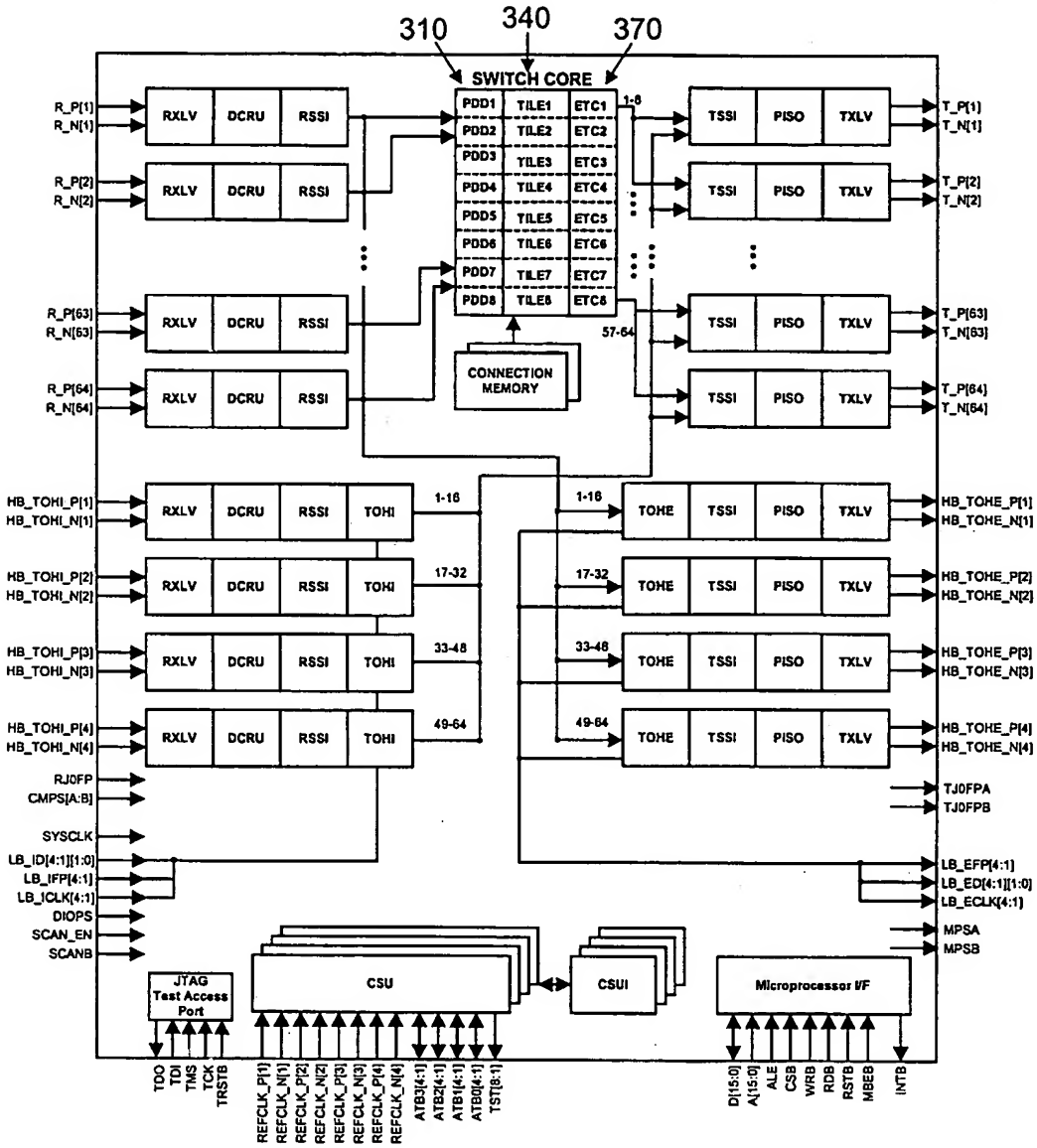

310
340
370
300
SWITCH CORE
CONNECTION MEMORY
RXLV
DCRU
RSSI
TOHI
TOHE
TSSI
PISO
TXLV
PDD1
PDD2
PDD3
PDD4
PDD5
PDD6
PDD7
PDD8
TILE1
TILE2
TILE3
TILE4
TILE5
TILE6
TILE7
TILE8
ETC1
ETC2
ETC3
ETC4
ETC5
ETC6
ETC7
ETC8
1-8
57-64
1-16
17-32
33-48
49-64
R_P[1]
R_N[1]
R_P[2]
R_N[2]
R_P[63]
R_N[63]
R_P[64]
R_N[64]
T_P[1]
T_N[1]
T_P[2]
T_N[2]
T_P[63]
T_N[63]
T_P[64]
T_N[64]
HB_TOHI_P[1]
HB_TOHI_N[1]
HB_TOHI_P[2]
HB_TOHI_N[2]
HB_TOHI_P[3]
HB_TOHI_N[3]
HB_TOHI_P[4]
HB_TOHI_N[4]
HB_TOHE_P[1]
HB_TOHE_N[1]
HB_TOHE_P[2]
HB_TOHE_N[2]
HB_TOHE_P[3]
HB_TOHE_N[3]
HB_TOHE_P[4]
HB_TOHE_N[4]
RJ0FP
CMPS[A:B]
SYSCLK
LB_ID[4:1][1:0]
LB_IFP[4:1]
LB_ICLK[4:1]
DIOPS
SCAN_EN
SCANB
TJ0FPA
TJ0FPB
LB_EFP[4:1]
LB_ED[4:1][1:0]
LB_ECLK[4:1]
MPSA
MPSB
JTAG Test Access Port
CSU
CSUI
Microprocessor I/F
TDO
TDI
TMS
TCK
TRSTB
REFCLK_P[1]
REFCLK_N[1]
REFCLK_P[2]
REFCLK_N[2]
REFCLK_P[3]
REFCLK_N[3]
REFCLK_P[4]
REFCLK_N[4]
ATB3[4:1]
ATB2[4:1]
ATB1[4:1]
ATB0[4:1]
TST[8:1]
D[15:0]
A[15:0]
ALE
CSB
WRB
RDB
RSTB
MBEB
INTB

FIG. 14